# BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

## IMAGES ARE BEST AVAILABLE COPY.

**As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.**

EP 18633 (3)

(12) UK Patent Application (19) GB (11) 2 306 778 (13) A

(43) Date of A Publication 07.05.1997

(21) Application No 9622642.8

(22) Date of Filing 30.10.1996

(30) Priority Data
(31) 07281602 (32) 30.10.1995 (33) JP

(71) Applicant(s)
NEC Corporation

(Incorporated in Japan)

7-1 Shiba 5-chome, Minato-ku, Tokyo 108-01, Japan

(72) Inventor(s)
Tatsuya Usami
Tatsuya Homma

(74) Agent and/or Address for Service
Mathys & Squire
100 Grays Inn Road, LONDON, WC1X 8AL,
United Kingdom

(51) INT CL$^6$
H01L 23/532

(52) UK CL (Edition O )
H1K KJAB K5BX K5B2 K5B3 K5B4 K5B9 K5C3G K5C3L

(56) Documents Cited
EP 0700087 A2 EP 0680085 A1 US 5521424 A
US 5512775 A

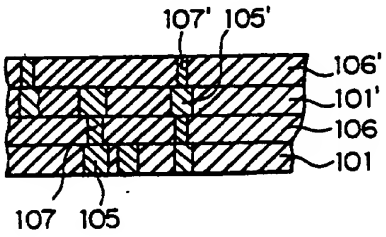
(58) Field of Search
UK CL (Edition O ) H1K KGFR KGFX KHAE KJAA KJAB KJAX
INT CL$^6$ H01L
Online:WPI,JAPIO,EDOC,INSPEC

# (54) Interlayer insulator

(57) An organic layer (101) of a resin which has a relative dielectric constant between 1.8 and 3.5 and which is selected from the group consisting of a polyimide resin and a fluororesin. The organic layer has a trench with a first metal (105) buried in the trench. A silicon oxide layer (106) containing fluorine (eg SiOF) is formed on the organic layer so that the silicon oxide layer has a hole above the first metal layer. A second metal (107) is buried in the hole. An additional organic layer (101') of the resin is formed on the silicon oxide layer so that the additional organic layer has an additional trench above the second metal. A further silicon oxide layer containing fluorine (106') may be formed on the resin layer (101').

The reduced dielectric constant of the composite interlayer insulating film reduces the parasitic capacitance and crosstalk between adjacent metallic conductors and interconnects.

FIG. 3J




GB 2 306 778 A

FIG. 1A
PRIOR ART

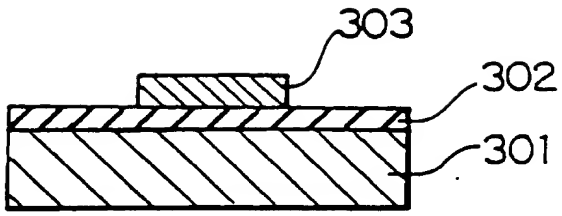



FIG. 1B
PRIOR ART

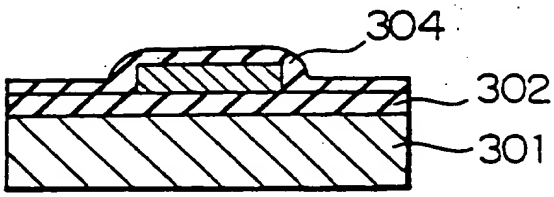



FIG. 1C
PRIOR ART

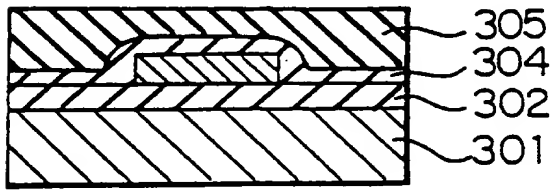



FIG. 1D
PRIOR ART

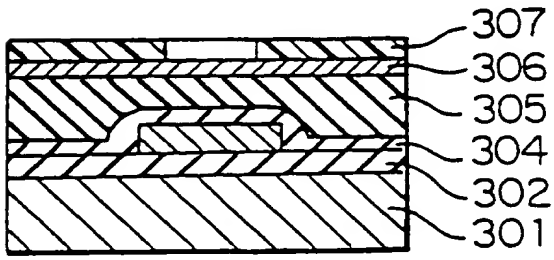


FIG. 1E
PRIOR ART

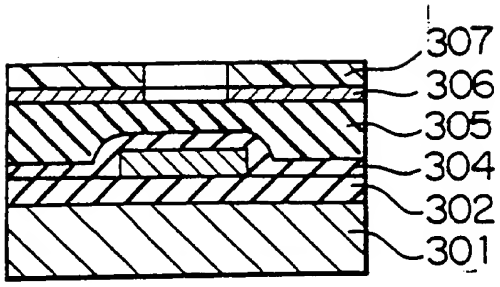



FIG. 1F
PRIOR ART

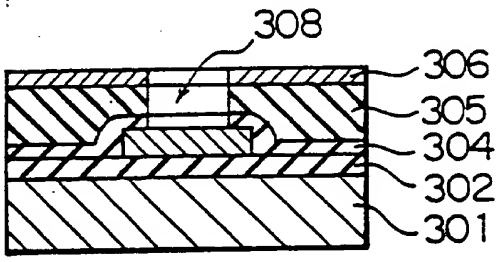



FIG. 1G
PRIOR ART

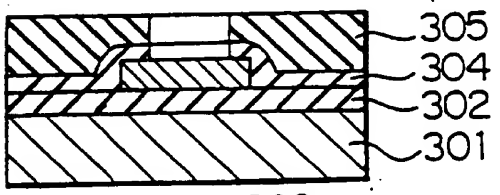
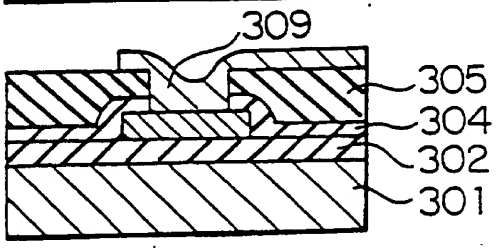



FIG. 1H
PRIOR ART



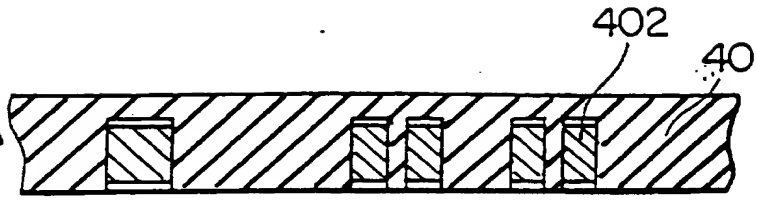



FIG. 2A
PRIOR ART

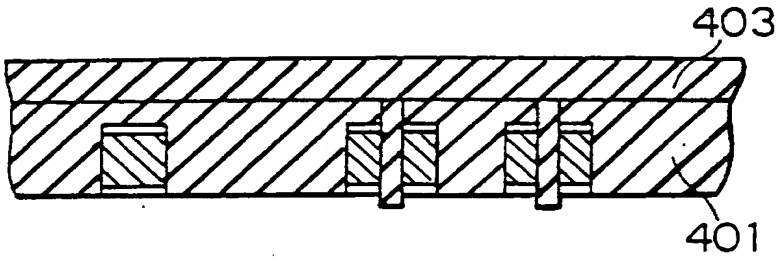



FIG. 2B
PRIOR ART

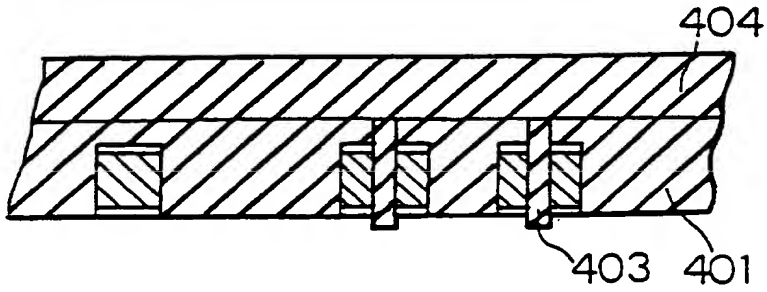



FIG. 2C
PRIOR ART

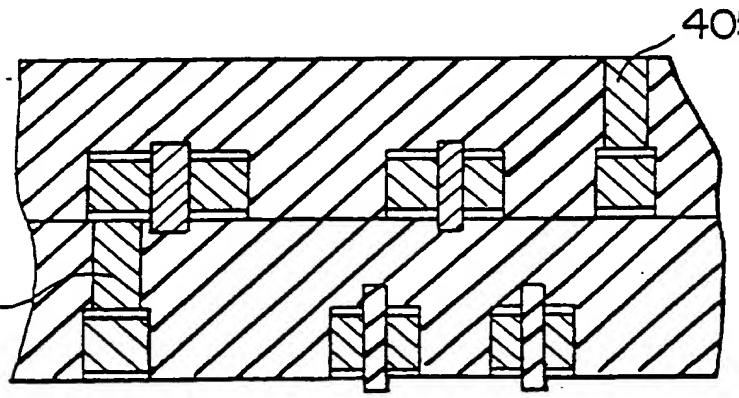



FIG. 2D
PRIOR ART

FIG. 4A


FIG. 4B

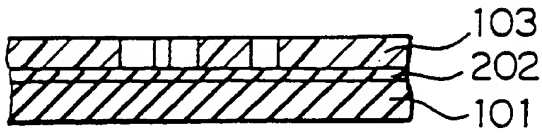



FIG. 4C

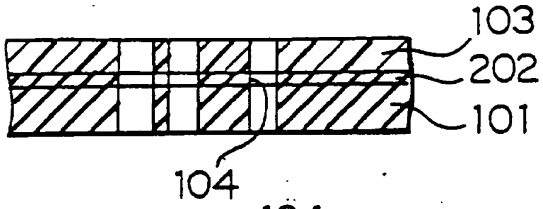



FIG. 4D

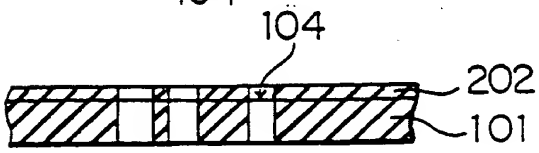



FIG. 4E

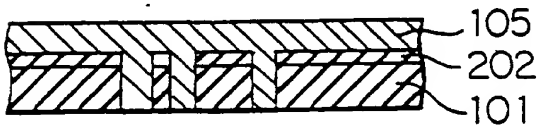


FIG. 4F

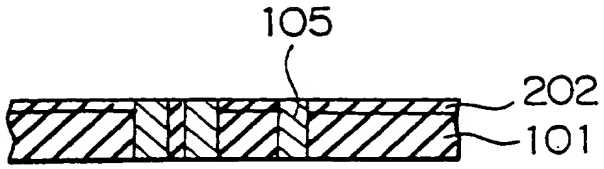



FIG. 4G

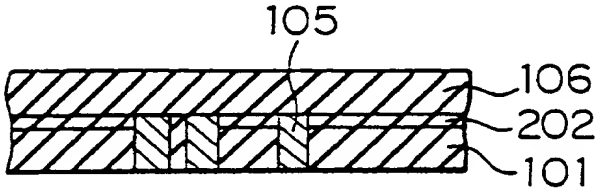



FIG. 4H

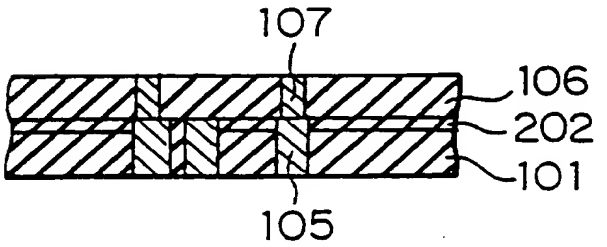



FIG. 4I

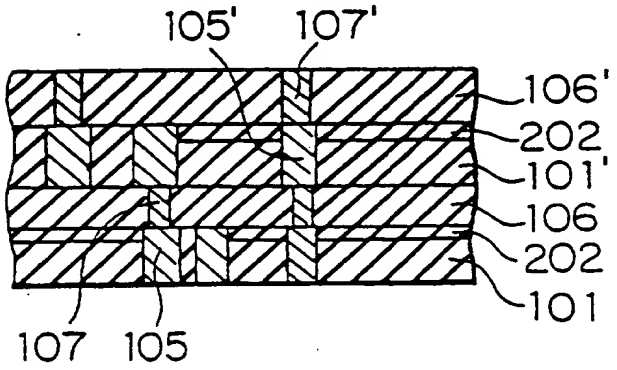


FIG. 3A

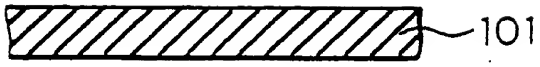



FIG. 3B

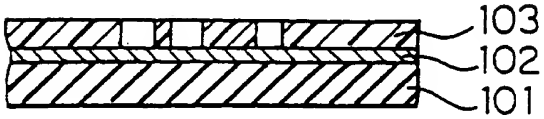



FIG. 3C

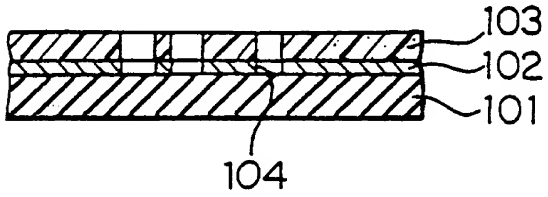



FIG. 3D

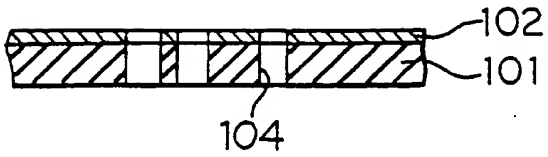



FIG. 3E

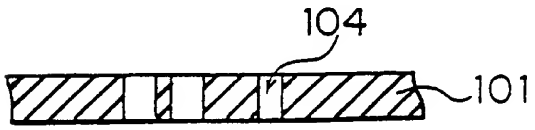



FIG. 3F

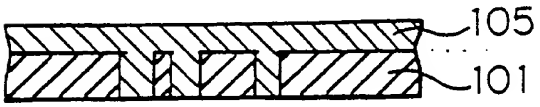


FIG. 3G

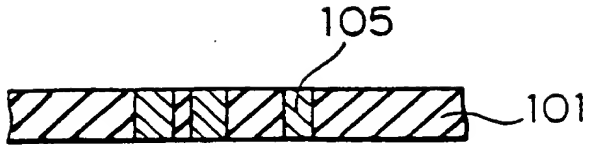



FIG. 3H

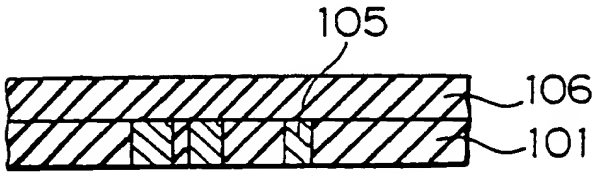



FIG. 3I

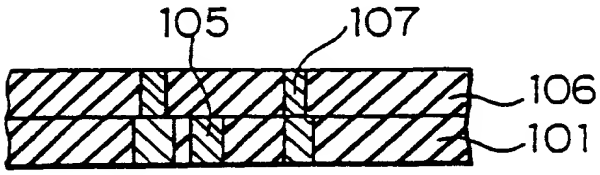
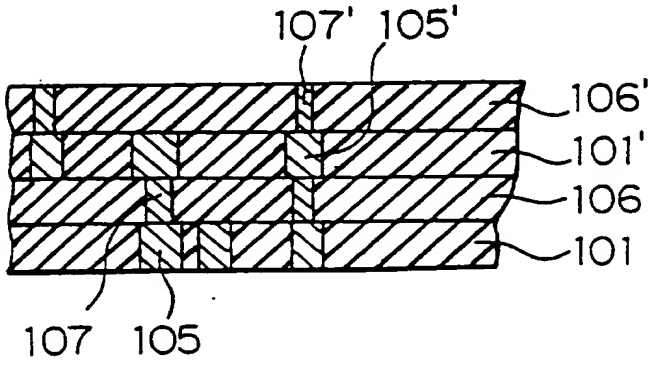



FIG. 3J



# SEMICONDUCTOR DEVICE AND A METHOD OF MANUFACTURING THE SAME

This invention relates to a semiconductor device of a multilevel or multilayer wiring structure. This invention also relates to a method of manufacturing the semiconductor device.

In recent years, a semiconductor integrated circuit becomes finer in structure. Such tendency is particularly remarkable in multilevel or multilayer wiring in a logic circuit. With an improvement in fineness of metal line spacing in the multilevel wiring, occurrence of crosstalk (a phenomenon that a signal on a line leaks onto an adjacent line) is inevitable between metal lines. In order to avoid occurrence of such crosstalk, it is proposed to use a low-dielectric-constant insulator layer as a line-to-line insulator layer between metal lines.

A technique of suppressing such crosstalk by using the low-dielectric-constant insulator layer is disclosed, for example, in an article written by Shin-Puu Jeng et al and entitled "A Planarized Multilevel Interconnect Scheme With Embedded Low-Dielectric-Constant

Polymers For Sub-Quarter-Micron Applications" contributed to 1994 Symposium on VLSI Technology Digest of Technical Papers, pp. 73-74. No effect is obtained unless a relative dielectric constant is equal to 3.5 or less.

In the current status, the relative dielectric constant is between 4 and 4.5 by the use of a P-SiO layer which is a SiO layer obtained by plasma chemical vapor deposition. It is therefore believed advantageous to use an organic layer having a relative dielectric constant between 1.8 and 3.5 instead of the P-SiO layer.

As one of the various known techniques using such organic layer, Japanese Unexamined Patent Publication No. 3-34558 (34558/1991) discloses a method of manufacturing a multilevel wiring structure. The method will herein be referred to as a first conventional method.

Another example of the various known techniques using the organic layer is disclosed in the above-mentioned Jeng et al article and will herein be referred to as a second conventional method.

Each of the first and the second conventional methods has various disadvantages which will later be described.

It is therefore an object of at least the preferred embodiments of the present invention to remove the disadvantages and to provide a semiconductor device of a multilevel wiring structure which is capable of preventing occurrence of crosstalk between metal lines.

It is another such object to remove the disadvantages and to provide a method of manufacturing a semiconductor device of a multilevel wiring structure which is capable of preventing occurrence of crosstalk between metal lines.

Accordingly, in a first aspect the present invention provides a semiconductor device comprising:

an organic layer comprising a resin having a relative dielectric constant in the range from 1.8 to 3.5 inclusive and selected from the group consisting of a polyimide resin and a fluororesin, said organic layer having a recess;

a first metallic member comprising a first metal and disposed in said recess;

a silicon oxide layer containing fluorine and disposed on said organic layer so as to have a hole disposed above said first metallic member; and

a second metallic member comprising a second metal and disposed in said hole.

In a second aspect, the present invention provides a method of manufacturing a semiconductor device, comprising the steps of:

preparing an organic layer comprising a resin having a relative dielectric constant in the range from 1.8 to 3.5 inclusive and selected from the group consisting of a polyimide resin and a fluororesin, said organic layer having a recess;

forming a first metallic member comprising a first metal in said recess;

forming a silicon oxide layer containing fluorine on said organic layer so that said silicon oxide layer has a hole disposed above said first metallic member; and

forming a second metallic member comprising a second metal in said hole.

Preferred features of the present invention will now be described, purely by way of example only, with reference to the accompanying drawings, in which:-

Figs. 1A through 1H are side sectional views for describing a succession of steps of a first conventional

method of manufacturing a semiconductor device;

Figs. 2A through 2D are side sectional views for describing a succession of steps of a second conventional method of manufacturing a semiconductor device;

Figs. 3A through 3J are side sectional views for describing a succession of steps of a method of manufacturing a semiconductor device according to a first embodiment of this invention; and

Figs. 4A through 4I are side sectional views for describing a succession of steps of a method of manufacturing a semiconductor device according to a second embodiment of this invention.

Referring to Figs. 1A through 1H, a first conventional method using an organic layer will first be described for a better understanding of this invention. The first conventional method is equivalent to the method disclosed in the above-referred Japanese Unexamined Patent Publication No. 3-34558 (34558/1991). Figs. 1A through 1H show a succession of steps of a multilevel wiring process required in manufacturing a two-level aluminum wiring structure according to the first conventional method.

Referring to Fig. 1A, a first aluminum line 303 having a thickness of about 1$\mu$m is formed on a semiconductor substrate 301 through an insulator layer 302. A polyimide-film-forming coating solution containing silicon is applied thereon by spin coating.

Thereafter, heat treatment is carried out for 30 minutes at 150℃ within an oven in a nitrogen gas atmosphere. Thus, a silicon-containing polyimide layer 304 having a thickness of about 0.2μm is formed as illustrated in Fig. 1B.

Subsequently, a dispersion of tetrafluoroethylene perfluoroalkyl vinyl ether copolymer is applied by spin coating. The dispersion is preliminarily prepared by forming fine particles of tetrafluoroethylene perfluoroalkyl vinyl ether copolymer with a diameter between 0.1 and 0.5 μm and dispersing the fine particles in pure water at a concentration of about 30 weight %. Then, heat treatment is carried out for ten minutes at 80℃ within an oven in a nitrogen gas atmosphere. Then, another heat treatment is carried out for ten minutes at 380℃ within an electric furnace in a nitrogen gas atmosphere to melt the fine particles. Thus, a fluororesin layer 305 of 1.3μm thick is formed as illustrated in Fig. 1C.

Subsequently, the surface of the fluororesin layer is exposed to argon gas plasma to be modified in quality within a sputtering apparatus. Successively within the same apparatus, a titanium layer 306 having a thickness of about 0.3μm is formed by sputtering and a photoresist layer 307 is then formed and patterned by a known photolithography technique, as illustrated in Fig. 1D. Thereafter, as illustrated in Fig. 1E, a hole is formed in the titanium layer 306 by reactive ion etching

using a mixture of $CCl_4$ gas and $SF_6$ gas. Subsequently, by reactive ion etching using a mixture of $O_2$ gas and $CF_4$ gas, a hole 308 is formed in the fluoro-resin layer and the silicon-containing polyimide layer simultaneously when the photoresist layer 307 is etched and removed, as illustrated in Fig. 1F.

Furthermore, immersion into an aqueous solution of a mixture of ammonium and hydrogen peroxide is carried out. As illustrated in Fig. 1G, an aluminum layer of about 1$\mu$m thick is formed by sputtering after the titanium layer 306 is removed. By the use of a known photoetching technique, a second aluminum line 309 is formed as illustrated in Fig. 1H. By repeating the above-mentioned steps, the multilevel wiring structure is formed.

Turning to Fig. 2A through 2D, a second conventional method using an organic layer will also be described for a better understanding of this invention. The second conventional method is equivalent to the method disclosed in the above-referred Jeng et al. article. Figs. 2A through 2D are side sectional views showing a succession of steps in a multilevel wiring process required in manufacturing a two-level wiring structure according to the second conventional method.

Referring to Fig. 2A, metal lines 402 are formed by etching and coated with an $SiO_2$ layer 401. Then, as illustrated in Fig. 2B, holes are formed in the $SiO_2$ layer 401 by etching narrow portions between the metal

lines 402. Thereafter, a polymer layer 403 having a low dielectric constant is deposited on the $SiO_2$ layer 401 and in the holes formed therein. Subsequently, as illustrated in Fig. 2C, the polymer layer 403 is etched to leave the polymer layer 403 only in the holes formed in the $SiO_2$ layer 401. An $SiO_2$ (overlayer) layer 404 is formed thereon. A hole is formed in the $SiO_2$ layer 404 as a through hole and a via 405 is buried in the hole. By repeating the above-mentioned steps, a multilevel wiring structure is formed as illustrated in Fig. 2D.

In the above-mentioned first conventional method, the silicon-containing polyimide layer 304 is inevitably exposed from the via hole 308 after the via hole 308 is formed. Inasmuch as the silicon-containing polyimide layer 304 is highly hygroscopic, interconnect resistivity of the aluminum line (metal line) 309 of the via hole 308 is increased when the silicon-containing polyimide layer 304 is exposed. As a result, the reliability of the metal line 309 is decreased.

On the other hand, in the above-mentioned second conventional method, the polymer layer 403 of a low dielectric constant is buried in the holes formed in the $SiO_2$ layer 401. Specifically, the polymer layer 403 must be buried in the holes having a high aspect ratio and is therefore restricted to be a high-coverage layer.

In addition, in the above-mentioned second conventional method, the $SiO_2$ layer 404 is used in order to coat the organic layer 403. Since $SiO_2$ has a relative

dielectric constant as relatively high as about 4, line-to-line capacitance in the vertical direction is increased. This results in decrease of a signal transmission speed between upper and lower metal layers.

In both of the first and the second conventional methods, the metal line has a selection ratio of the order of 3 with respect to the photoresist layer. Accordingly, the fine wiring process is restricted by the accuracy in patterning the photoresist layer. It is therefore difficult to accurately and finely form the metal line so that a prospective ultrafine multilevel wiring structure is achieved.

This invention removes the above-mentioned disadvantages. That is, this invention is to provide a semiconductor device of a multilevel wiring structure which is capable of preventing occurrence of crosstalk between metal lines, increase in interconnect resistivity due to moisture absorption of an interlayer insulator layer, and metal corrosion and which is highly integrated in embedding ability of the interlayer insulator layer, and to provide a method of manufacturing the semiconductor device.

Figs. 3A through 3J show a method of manufacturing a semiconductor device according to a first embodiment of this invention.

Referring to Fig. 3J, description will briefly be made as regards a structure of the semiconductor device. The semiconductor device includes an organic layer 101 of

a resin which has a relative dielectric constant between 1.8 and 3.5, both inclusive, and which is selected from the group consisting of a polyimide resin and a fluoro-resin. The organic layer 101 has a slit which will be called a trench in the art. A first metal 105 is buried in the slit as a metal line. A fluorine-containing silicon oxide layer 106 containing fluorine is formed on the organic layer 101 so as to have a hole on the first metal 105. A second metal 107 is buried in the hole.

An additional organic layer 101' of the resin is formed on the fluorine-containing silicon oxide layer 106 so as to have an additional slit on the second metal 107. A first additional metal 105' is buried in the additional slit as an additional metal line. An additional fluorine-containing silicon oxide layer 106' containing fluorine is formed on the additional organic layer 101' so as to have an additional hole on the first additional metal 105'. A second additional metal 107' is buried in the additional hole.

The organic layer 101 is formed first and then the slit is formed therein by, for example, reactive ion etching. Thereafter, the first metal 105 is buried in the slit. The fluorine-containing silicon oxide layer 106, which is less hygroscopic, is formed thereon. Thereafter, the hole is formed on the first metal 105. Thus, the organic layer 101 is never exposed at the hole so as to prevent increase in interconnect resistivity of the second metal 107 of the hole and corrosion of the

second metal 107. In addition, since the organic layer 101 is formed first, embedding ability of the organic layer 101 in not restricted and the reliability of the device is not degraded. Since the fluorine-containing silicon oxide layer 106 having a relatively high dielectric constant is deposited on the organic layer 101, the line-to-line capacitance in the vertical direction is suppressed to be small so that the decrease in signal processing speed is hardly caused to occur. In addition, the first metal 105 is buried in the slit according to the above-mentioned steps. Therefore, the accuracy of the fine wiring process is further improved beyond the accuracy in forming the organic layer because the selection ratio with respect to the photoresist layer is saved.

Now, description will be made in detail as regards a method of manufacturing the semiconductor device according to the first embodiment of this invention with reference to Figs. 3A through 3J.

Referring to Fig. 3A, a fluororesin layer 101 having a relative dielectric constant between 1.8 and 3.0 was deposited on a semiconductor substrate (not shown) by spin coating to a thickness of about 7000 angstroms. Baking was carried out for ten minutes in an $N_2$ atmosphere at a temperature between 300 and 400℃. Thereafter, the surface of the fluororesin layer 101 was exposed to argon gas plasma within a sputtering apparatus and was modified in quality. Then, successively in the

same apparatus, a titanium layer 102 of 3000 angstroms thick was formed by sputtering, as illustrated in Fig. 3B.

Next, by the use of a known photolithography technique, a photoresist layer 103 was patterned as illustrated in Fig. 3B. Then, slits 104 were formed in the titanium layer 102 by reactive ion etching using a mixture of $CCl_4$ gas and $SF_6$ gas, as illustrated in Fig. 3C.

Subsequently, by reactive ion etching using a mixture of $O_2$ gas and $CF_4$ gas, the slits 104 were formed in the fluororesin layer 101 simultaneously when the photoresist layer 103 was etched and removed, as illustrated in Fig. 3D.

Then, dipping into an aqueous solution of a mixture of ammonium and hydrogen peroxide was carried out to remove the titanium layer 102 as illustrated in Fig. 3E. Thereafter, as illustrated in Fig. 3F, a blanket Cu layer (a first metal) 105 was deposited on the fluororesin layer 101 and the slits 104 to have a thickness of about 1$\mu$m on the fluororesin layer 101.

Furthermore, chemical mechanical polishing (CMP) was carried out for planarization to leave the Cu layer 105 only in the slits as illustrated in Fig. 3G. Thereafter, a fluorine-containing silicon oxide layer 106 containing 2-15 wt% of fluorine was formed by high-density plasma CVD using $SiF_4$ gas, $O_2$ gas, and Ar gas, as illustrated in Fig. 3H.

Subsequently, by the use of a known photolithography technique, another photoresist layer 103 was formed and patterned. Then, by reactive ion etching using a mixture of $CF_4$ gas and $O_2$ gas, holes were formed in the fluorine-containing silicon oxide layer 106. Thereafter, the photoresist layer 103 was removed and Al plugs (second metal) 107 were grown within the holes, as illustrated in Fig. 3H. By repeating these steps, a multilevel wiring structure is formed as illustrated in Fig. 3J.

Turning to Figs. 4A through 4I, description will be made as regards a method of manufacturing a semiconductor device according to a second embodiment of this invention.

The second embodiment is different from the first embodiment in that the metal layer (titanium layer 102) used as a mask member in the step of forming the slits 104 in the fluororesin layer 101 is replaced by a fluorine-containing silicon oxide layer 202. A resultant advantage is that the mask member is left unremoved and therefore the steps of removing the metal and etching a single layer of the fluororesin layer 101 in the first embodiment can be omitted. In the first embodiment, the accuracy is insufficient upon finely patterning the mask because the metal layer has a selection ratio as small as about 3 with respect to the photoresist layer. In the second embodiment on the other hand, a photoresist layer for an insulator layer has a selection ratio as large as

between 7 and 8 so that the accuracy is improved.

In the second embodiment, the fluororesin layer 101 was formed first and baking was then carried out to form a structure illustrated in Fig. 4A. Thereafter, a fluorine-containing silicon oxide layer 202 was deposited to a thickness of 3000 angstroms as illustrated in Fig. 4B.

Next, by the use of a known photolithography technique, the photoresist layer 103 was patterned as illustrated in Fig. 4B. Thereafter, a stack of the fluorine-containing silicon oxide layer 202 and the fluororesin layer 101 were simultaneously patterned by reactive ion etching using a mixture of $O_2$ gas and $CF_4$ gas to form the slits 104 as illustrated in Fig. 4C. Subsequently, as illustrated in Fig. 4D, the photoresist layer 103 alone was removed. Then, the steps in Figs. 4E through 4H were carried out which are similar to the step in Figs. 3F through 3I in the first embodi-ment. Finally, by repeating the above-mentioned steps, a multilevel wiring structure having Cu layers (first metals) 105 and Al plugs (second metals) 107 was formed as illustrated in Fig. 4I.

In the first and the second embodiments described above, the fluororesin layer 101 is used as the organic layer. Alternatively, a polyimide resin layer can be used. As the mask member to form the grooves in the organic layer, use is made of the titanium layer 102 in the first embodiment. Alternatively, use may be made of

at least one of various metal layers including a tungsten layer, a titanium-containing tungsten layer, a molybdenum layer, an aluminum layer, and an aluminum alloy layer. In the second embodiment, the fluorine-containing silicon oxide layer 202 is used. Instead, use may be made of at least one of various inorganic layers, including a silicon oxide layer, a silicon nitride layer, and a silicon oxide nitride layer, formed by plasma chemical vapor deposition or sputtering. In addition, the surface of the organic layer such as the fluororesin layer may be modified by the use of reactive ion etching using $CF_4$ gas or $O_2$ gas.

On the other hand, attention will be directed to the first metals 105 and 105' and the second metals 107 and 107'. In the first and the second embodiments, the Cu layer is used as the first and the second metals 105, 105', 107, and 107', respectively. It is noted here that each of Cu and Al can be used for either of the first and the second metals. Alternatively, a different metal layer such as W, Au, or the like can be used. In order to improve the reliability of the first and second metals, Pd, Cu, Si, and the like can be included. In addition, depending upon the metal material, a single layer of Ti, TiN, TiW, or poly-Si or a combination thereof can be used as a barrier layer.

On the other hand, in order to form the organic layers 101 and 101', the first and the second embodiments adopt spin coating followed by baking. Instead,

deposition by plasma CVD can be used. In the first and the second embodiments, each of the fluorine-containing silicon oxide layers 106 and 106' is formed by the high-density plasma CVD using $SiF_4$ gas, $O_2$ gas, and Ar gas. Instead, parallel-plate plasma CVD may be used. In addition, the $SiF_4$ may be replaced by a combination of $SiH_4$ and an additive gas selected from $C_2F_6$, $CF_4$, $NF_3$, and $SF_6$, or a combination of TEOS (tetra-ethyl orthosilicate) and an additive gas selected from $C_2F_6$, $CF_4$, $NF_3$, and $SF_6$. Alternatively, FTES (fluorotriethoxy silane) may be used. It is noted here that $O_2$ can be replaced by one of $N_2O$, NO, $CO_2$, CO, $O_3$, and $H_2O$ and that Ar is not necessarily be added.

As described above, in the semiconductor device and the method of manufacturing the same according to this invention, it is possible to prevent occurrence of crosstalk between the metal lines, increase in interconnect resistivity due to moisture absorption of an interlayer insulator, and metal corrosion and to improve the reliability with the highly integrated embedding ability of the interlayer layer. These advantages will hereafter be specifically mentioned.

(1) The multilevel wiring structure without exposure of the organic layer at the via hole effectively prevents increase in interconnect resistivity of the via hole. Therefore, the reliability of the metal lines is improved.

(2) Since the organic layer is formed prior to formation of the metal lines, the hole metal structure need not be adopted to improve embedding ability of the organic layer. It is therefore possible to prevent decrease in reliability of the device due to occurrence of void.

(3) Because the SiOF layer is interposed between the metals in the vertical direction, the relative dielectric constant is decreased to a value between 3.0 and 3.7 (between 4 and 4.5 with the $SiO_2$ layer used in the above-mentioned another conventional example). Therefore, a delay is present in signal processing speed between the upper and the lower metal lines so that about 10% decrease of crosstalk is realized when a line width is equal to 0.6$\mu$m for example.

(4) Since the organic layer is formed prior to formation of the metal lines and the groove is thereafter formed, the margin is further widened. This is because the limit in finely processing the insulator layer is superior as compared with the metal line. Accordingly, very fine metal lines can be formed without taking the limit in metal processing into consideration.

It will be understood that the present invention has been described above purely by way of example, and modifications of detail can be made within the scope of the invention.

Each feature disclosed in the description, and (where appropriate) the claims and drawings may be provided independently or in any appropriate combination.

In summary, on manufacturing a semiconductor device, preparation is made of an organic layer of a resin which has a relative dielectric constant between 1.8 and 3.5, both inclusive, and which is selected from the group consisting of a polyimide resin and a fluororesin. The organic layer has a slit. A first metal is buried in the slit. A silicon oxide layer containing fluorine is formed on the organic layer so that the silicon oxide layer has a hole on the first metal. A second metal is buried in the hole. Preferably, an additional organic layer of the resin is formed on the silicon oxide layer so that the additional organic layer has an additional slit on the second metal. In this case, a first additional metal is buried in the additional slit. In addition, an additional silicon oxide layer containing fluorine may be formed on the additional organic layer so that the additional silicon oxide layer has an additional hole on the first additional metal. In this event, a second additional metal is buried in the additional hole.

CLAIMS

1. A semiconductor device comprising:

an organic layer comprising a resin having a relative dielectric constant in the range from 1.8 to 3.5 inclusive and selected from the group consisting of a polyimide resin and a fluororesin, said organic layer having a recess;

a first metallic member comprising a first metal and disposed in said recess;

a silicon oxide layer containing fluorine and disposed on said organic layer so as to have a hole disposed above said first metallic member; and

a second metallic member comprising a second metal and disposed in said hole.

2. A semiconductor device as claimed in Claim 1, further comprising:

an additional organic layer comprising said resin, said additional organic layer being disposed on said silicon oxide layer so as to have an additional recess disposed above said second metallic member; and

a third metallic member comprising said first metal and disposed in said additional recess.

3. A semiconductor device as claimed in Claim 2, further comprising:

an additional silicon oxide layer containing fluorine and disposed on said additional organic layer so as to have an additional hole disposed above said third metallic member; and

a fourth metallic member comprising said second metal and disposed in said additional hole.

4. A method of manufacturing a semiconductor device, comprising the steps of:

preparing an organic layer comprising a resin having a relative dielectric constant in the range from 1.8 to 3.5 inclusive and selected from the group consisting of a polyimide resin and a fluororesin, said organic layer having a recess;

forming a first metallic member comprising a first metal in said recess;

forming a silicon oxide layer containing fluorine on said organic layer so that said silicon oxide layer has a hole disposed above said first metallic member; and

forming a second metallic member comprising a second metal in said hole.

5. A method of manufacturing a semiconductor device as claimed in Claim 4, wherein said preparing step comprises the steps of:

forming said organic layer by spin coating; and

subjecting said organic layer to heat treatment.

6. A method of manufacturing a semiconductor device as claimed in Claim 4, wherein said preparing step comprises the step of:

forming said organic layer by plasma chemical vapour deposition.

7. A method of manufacturing a semiconductor device as claimed in Claim 4, wherein said step of forming said silicon oxide layer comprises the step of:

forming said silicon oxide layer by plasma chemical vapour deposition.

8. A method as claimed in any of Claims 4 to 7, further comprising the steps of:

forming an additional organic layer comprising said resin on said silicon oxide layer so that said additional organic layer has an additional recess disposed above said second metallic member; and

forming a third metallic member comprising said first metal in said additional recess.

9. A method of manufacturing a semiconductor device as claimed in Clam 8, wherein said step of forming said additional organic layer comprises the steps of:

forming said additional organic layer by spin coating; and

subjecting said additional organic layer to heat treatment.

10. A method of manufacturing a semiconductor device as claimed in Claim 8, wherein said step of forming said additional organic layer comprises the step of:

forming said additional organic layer by plasma chemical vapour deposition.

11. A method as claimed in any of Claims 8 to 10 further comprising the steps of:

forming an additional silicon oxide layer containing fluorine on said additional organic layer so that said additional silicon oxide layer has an additional hole disposed above said third metallic member; and

forming a fourth metallic member comprising said second metal in said additional hole.

12. A method of manufacturing a semiconductor device as claimed in Claim 11, wherein said step of forming said additional silicon oxide layer comprises the step of:

forming said additional silicon oxide layer by plasma chemical vapour deposition.

13. A semiconductor device substantially as herein described with reference to and as shown in Figure 3I or Figure 3J or Figure 4H or Figure 4I of the accompanying drawings.

14. A method of manufacturing a semiconductor device substantially as herein described with reference to Figures 3A to 3I or Figures 4A to 4H of the accompanying drawings.

The Patent Office

21

**Application No:** GB 9622642.8 **Examiner:** SJ Morgan
**Claims searched:** 1-14 **Date of search:** 13 January 1997

## Patents Act 1977
## Search Report under Section 17

**Databases searched:**

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.O): H1K(KGFR,KGFX,KHAE,KJAA,KJAB,KJAX)

Int Cl (Ed.6): H01L

Other: Online:WPI,JAPIO,EDOC,INSPEC

**Documents considered to be relevant:**

| Category | Identity of document and relevant passage | | Relevant to claims |
|---|---|---|---|
| A,P | EP 0 700 087 A2 | (TOSHIBA) See whole document. | |
| A,P | EP 0 680 085 A1 | (TEXAS INSTRUMENTS) See table and figures. | |
| A,P | US 5 521 424 | (NEC) See whole document. | |
| A,P | US 5 512 775 | (TEXAS INSTRUMENTS) See table and figures. | |

| | | | |
|---|---|---|---|
| X | Document indicating lack of novelty or inventive step | A | Document indicating technological background and/or state of the art. |
| Y | Document indicating lack of inventive step if combined with one or more other documents of same category. | P | Document published on or after the declared priority date but before the filing date of this invention. |
| & | Member of the same patent family | E | Patent document published on or after, but with priority date earlier than, the filing date of this application. |